REMARKS

Claim Objections

The Examiner had objected to claims 4-6 as being dependent on cancelled claim 2. Claim 4 has been amended to depend from claim 1 and therefore claims 5 and 6 now have the correct dependency.

Claim Rejection Section 112

The Examiner had rejected Claims 1, 4 -21 as being indefinite because of the recitation that the second clock signal is "directly connected to ground through a resistor". Claim 1 has been amended to recite that the second clock signal is transmitted to ground through a resistor, the second signal wire being a direct current connection to ground through the resistor.

The Examiner had noted similar language in claim 10. Claim 10 has been similarly amended.

Accordingly, claims 1, 4 -21 should now comply with Section 112.

Claim Rejection Section 103

The examiner had rejected claims 1, 4-21 as being unpatentable over US 5,811,837 to Misawa in view of US 6,198,307 to Garlepp. Garlepp teaches a differential driver 15 and a pair of differential clock lines 18 and 19 tied together at their ends by terminating resistors RT1 and RT2. The junction of terminating resistors RT1 and RT2 is labeled Ch_mid in Fig. 9 and may optionally have an AC ground (capacitance C_{END}). Garlepp explains this connection at col. 7 lines 53-57):

> Assuming the signals CTM and CTMN are truly differential, i.e., the signals are 180 degrees out-of-phase with each other, the node Ch_mid will appear as a differential ground with the conductors 18 and 19 being terminated with the termination resistors RT1 and RT2 * * * [which] prevent reflections of the differential signals CTM and CTMN * * * (Emphasis added).

Garlepp is thus seen to teach differential drive lines 18, 19 connected to a *differential* ground node Ch_mid which is optionally allowed to have an "AC ground", Garlepp Col. 3, lines 15-18.

Thus understood, Garlepp drive lines 18, 19 are similar to the Misawa drive lines 218, 219, which Misawa points out exhibit parasitic capacitances C_{s1} through C_{s4} with respect to video signal line 217. Misawa attempts to compensate for the parasitic capacitances between each of the drive lines and signal line 217 by twisting the drive lines 218, 219.

The Examiner's thoughts that the Misawa and Garlepp teachings can be combined would have the effect of connecting the ends of Misawa's drive lines 218, 219 with Garlepp's impedance matching resistors RT1 and RT2 to an AC ground, i.e., a capacitor, such as C_{END}.

However, capacitor at the ends of the transmission lines would fail to compensate for electromagnetic interference (EMI) for the same reason that the parasitic capacitances of the lines themselves accumulate charges that are a cause of EMI. EMI, as explained by applicant at pages 10-11 is:

> * * * typically generated in TFT-ICDs during the transmission of high frequency signals from a strip-type high frequency wire and a ground surface area adjacent to this wire. The

> electric field generated between the high frequency wire and the ground surface area accumulates in the ground surface area electric charges with a polarity opposite to the high frequency wire. The strength of EMI is directly proportionate to the current flowing on the ground surface, which depends on the movement of the electric charges. Therefore, EMI can be reduced by minimizing the amount of the current fluctuation on the ground surface.

The reduction of EMI by minimizing current fluctuation on the ground surface is achieved by applicant, as explained at p.10, by a DC ground, as follows:

> Referring to FIG. 5, when transmitting the first shift clock signal CIK1 to the data driver ICs 200a, 200b, 200c and 200d, a second shift clock signal CIK2, which has the same frequency as the first shift clock signal CIK1 but has an opposite phase is sent to a ground GND via a resistor Re to minimize EMI caused by the transmission of the first shift clock signal CIK 1. A dummy wire is provided on the first PCB 500 parallel to the wire used for the first shift clock signal CIK1, and the second shift clock signal CIK2 is output from the timing controller 550 to the ground GND through the dummy wire to offset the EMI caused by the transmission of the first shift clock signal CIK1.

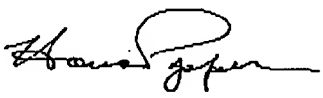
The combination of Misawa and Garlepp as the Examiner proposed, i.e., using an AC ground capacitor would not alter the deleterious effect on EMI of parasitic capacitance from a clock drive line to an adjacent *ground surface area*.

Claim 1 has been amended to specify that the first signal wire is

adjacent to a ground surface area through which the shift clock signal is transmitted to the data drivers and that the second signal wire is a direct current connection to the ground surface area through a resistor.

Accordingly, Claims 1, 4-21variously dependent on claim 1 distinguish over the combination of references suggested by the Examiner and applicants therefore respectfully request the withdrawal of the rejection of Claims 1, 4-21.

Respectfully submitted,



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Attorney for Applicants 7/31/2007 Date

Howard R. Popper
Reg. No. 19,208
MacPherson Kwok Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
408-392-9250